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10/781,657	02/20/2004	Takanori Ishii	1075.1250	3472

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EXAMINER	
SCHELL, JOSEPH O	
ART UNIT	**PAPER NUMBER**
2114	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,657	ISHII, TAKANORI	
	Examiner	Art Unit	
	Joseph Schell	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8,9,12,13,16,17,20,21,24,25,28,29,32,33 and 36* is/are rejected.

7)☒ Claim(s) *2,3,6,7,10,11,14,15,18,19,22,23,26,27,30,31,34 and 35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-36 have been examined.

Claims 2-3, 6-7,10-11, 14-15, 18-19, 22-23, 26-27, 30-31, and 34-35 have been objected to as containing allowable subject matter, yet dependant upon rejected base claims.

Claims 1, 4-5, 8-9, 12-13, 16-17, 20-21, 24-25, 28-29, 32-33 and 36 have been rejected.

Information Disclosure Statement

1. The IDS submitted February 20, 2004 says that a translation of claim 1 for JP 61-196353 has been submitted. However, this translation was either omitted or lost and is not presently available in with file for the examiner to review.

Claim Objections

2. Claim 1 line 15, Claim 3 line 7, Claims 9-12 line 10, Claim 13 line 33, Claim 14 line 5, Claim 15 line 6, line 9 of Claims 21-24, line 33 of Claim 25, line 6 of Claim 27, and Claims 33-36 line 10 use the phrasing "notifies of said error" or "notifying of said error". Without explicit identification of a target of the notification this wording is awkward. A change to "sends said error notice" or "transmits said error notice" is suggested.

3. Claim 1 line 8, Claim 13 line 25, and Claim 25 line 25 state "a basic mode predetermined between said at least two" and should instead read "a basic mode predetermined to be one of said at least two".

4. Claim 13 line 11 should read "a bridge module connected to said disk". Claim 13 line 13 should read "through interface buses; said bridge module connecting said disk interface..."

Specification

5. Page 12 lines 2-3 of the specification should read "specifically adding to or/and changing the hardware.."

Allowable Subject Matter

6. Claims 2-3, 6-7,10-11, 14-15, 18-19, 22-23, 26-27, 30-31, and 34-35 are objected to as containing allowable subject matter yet dependent on rejected base claims.

Within the Claims stated above, the examiner deems the novel limitation to be, within the entirety of the claim, the rerunning of the mode setting sequence in response to the error notice from the notifying means (wherein said notice indicates a mode mismatch).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Holley (US Patent 6,954,813).

8. As per claim 1, Holley ('813) discloses an apparatus having a transfer mode abnormality detecting function comprising:

at least two modules connected to each other through an interface bus in at least two different modes so that data can be transferred between said modules (as shown in Figure 1, the Hotplug devices 150 in hotplug slots 1 and 2 are connected to common bus B, they are also connected to a PCI bridge controller 134);

a determining means for determining whether or not a basic mode predetermined between said at least two different modes agrees with a mode set in a mode setting sequence executed when said apparatus is reset or when data is transferred between said modules (column 5 lines 46-49, an error occurs when a slower device is added to the same bus as a faster device; the mode is the faster PCI bus speed, previously agreed upon by the faster PCI device and the bridge controller); and

a notifying means for determining that transfer mode abnormality occurs when said determining means determines that said modes do not agree with each other, and for notifying of an error notice (column 7 lines 1-5).

9. As per claim 5, Holley ('813) discloses the apparatus having a transfer mode abnormality detecting function according to claim 1, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus (column 3 lines 33-35).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 4-5, 8-9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohwada (US Patent 7,003,701) in view of Sciforums and PC Hardware.

11. As per Claim 1, Ohwada ('701) discloses an apparatus having a transfer mode abnormality detecting function (see abstract) comprising:

at least two modules connected to each other through an interface bus in at least two different modes so that data can be transferred between said modules (as shown in Figure 1, multiple PCI devices exist on a PCI bus 10, functionally connected to the

processor and memory via a host bridge. The PCI specification revision 2.3 outlines the PCI use of 64-bit and 32-bit transfers. While 64-bit transfer is useful for products needing more bandwidth (PCI Specification section 3.8) 64-bit PCI devices are also capable of transfer in 32-bit mode for backward compatibility (PCI Specification section 3.8))

a determining means (as shown in Figure 1, the PCI bus monitor circuit 200);

a mode set in a mode setting sequence executed when said apparatus is reset or when data is transferred between said modules (PCI specification revision 2.3 section 3.8, 64-bit transactions are dynamically negotiated once per transmission); and

a notifying means for determining that transfer mode abnormality occurs when said determining means determines an error occurs, and for notifying of an error notice (see abstract, when plural PCI devices respond to a target address the processor is notified of an error).

Ohwada ('701) discloses a system that detects a transfer error stemming from too many devices accepting a communication. And while Ohwada ('701) does feature a PCI device that would be obvious to have 64-bit and 32-bit transfer modes (32-bit mode being used on the occurrence of a 64-bit mode setup discrepancy), Ohwada ('701) does not expressly disclose the system wherein an error occurs upon a transfer mode discrepancy. In the claim language, Ohwada ('701) does not expressly disclose the system wherein the PCI bus monitor reports an error upon determining that a basic

mode predetermined between said at least two different mode does not agree with a mode set in a mode setting sequence.

Sciforums teaches the use of a TV/Video Capture Card and that a lower level of service (dropped frames) can result from a number of system deficiencies, one of which is transfer rate.

PC Hardware in a Nutshell section 11.4 teaches that original CD burning suffered from buffer underrun errors that resulted in a failed burned CD when a data stream to the CD burner is interrupted long enough for the burner to write through all the data in its buffer.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the PCI bus monitoring system disclosed by Ohwada ('701) such that it detects the use of the stunted 32-bit transfer mode instead of a 64-bit mode and raises a fault. This modification would have been obvious because many applications, such as CD burning and video capture require a minimum transfer rate, below which an error or decreased quality of service occurs.

12. As per claim 4, Ohwada ('701) in view of Sciforums and PC Hardware discloses the apparatus having a transfer mode abnormality detecting function according to claim 1, wherein said determining means determines that said modes do not agree with each other when a confirmation signal responding to said basic mode remains disabled at the

time of executing said mode setting sequence (this is how PCI works, see PCI specification revision 2.3 section 3.8. REQ64 and ACK64 signals are sent by the receiver and transmitter. A lack of response with ACK64 on the part of the receiver causes the transmission to be downgraded to 32-bit mode).

13. As per claim 5, Ohwada ('701) in view of Sciforums and PC Hardware discloses the apparatus having a transfer mode abnormality detecting function according to claim 1, wherein said interface bus is a PCI (Peripheral Component Interconnect) bus (Ohwada Figure 1).

14. As per claim 8, this claim recites limitations found collectively in claims 4 and 5 and is rejected on the same grounds as claims 4 and 5.

15. As per claim 9, Ohwada ('701) in view of Sciforums and PC Hardware discloses the apparatus having a transfer mode abnormality detecting function according to claim 5, wherein

said interface bus is a 64-bit PCI bus (as disclosed by Ohwada's ('701) use of PCI buses and PCI specification 2.3's use of 64-bit bus),

said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8),

said basic mode is said 64-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8, the 64-bit transfer mode provides additional bandwidth an is thus the preferred transfer mode); and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality (this limitation is made obvious by Sciforums and PC Hardware, in which a lower transfer rate results in an error or reduced quality of service), and notifies of said error notice (in Ohwada ('701) the bus monitor forwards a notice to the processor when a PCI bus error occurs).

16. As per claim 12, this claim recites limitations found collectively in claims 8 and 9 and is rejected on the same grounds as claims 8 and 9.

17. Claims 13, 16, 17, 20, 21, 24, 25, 28, 29, 32, 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Garbus (US Patent 5,884,027) in view of Sciforums and PC Hardware in a Nutshell.

18. As per claim 13, Garbus ('027) discloses a storage controlling apparatus disposed between a disk unit and a host to control an access from said host to said unit, said storage controlling apparatus comprising:

a disk interface module for controlling an interface with said disk unit (Figure 2, elements 23 are SCSI controllers for storage devices);

a host interface module for controlling an interface with said host (as shown in Figure 2, the Processors 1-4 on the left are on a PCI bus (indicated by the PCI-to-PCI bridge 31), this necessitates the processors include a PCI interface);

a management module for generally managing the whole of said apparatus (the processor residing in the PCI-to-PCI bridge 31 operates as an address filter (column 6 lines 33-35);

a bridge module connected said disk interface module, said host interface module and said management module through interface buses to connect said disk interface module, said host interface module and said management module to one another so that data can be transferred among said disk interface module, said host interface module and said management module (as shown in Figure 2, the bridge, SCSI storage devices, and host processors 1-4 are connected via PCI buses);

said disk interface module, said host interface module, said management module and said bridge module being connected in at least two different modes so that data can be transferred among said disk interface module, said host interface module, said management module and said bridge module (as shown in Figure 2, the system employs a PCI bus. The PCI specification revision 2.3 outlines the PCI use of 64-bit and 32-bit transfers. While 64-bit transfer is useful for products needing more bandwidth (PCI Specification section 3.8) 64-bit PCI devices are also capable of transfer in 32-bit mode for backward compatibility (PCI Specification section 3.8));

a determining means an error (column 8 lines 36-38, configuration registers of the bridge module hold error condition information); and

a notifying means for determining that mode abnormality occurs when said determining means determines an error (for example, column 17 lines 18-26, a parity error is detected and reported).

Garbus ('027) discloses a system that detects a bus parity error for data transmitting across the bridge. And while Garbus ('027) does feature a PCI device that would be obvious to have 64-bit and 32-bit transfer modes (according to the PCI specification, the 32-bit mode being used on the occurrence of a 64-bit mode setup discrepancy), Garbus ('027) does not expressly disclose the system wherein an error occurs upon a transfer mode discrepancy. In the claim language, Garbus ('027) does not expressly disclose the system wherein the PCI bus monitor reports an error upon determining that a basic mode predetermined between said at least two different mode does not agree with a mode set in a mode setting sequence.

Sciforums teaches the use of a TV/Video Capture Card and that a lower level of service (dropped frames) can result from a number of system deficiencies, one of which is transfer rate.

PC Hardware in a Nutshell section 11.4 teaches that original CD burning suffered from buffer underrun errors that resulted in a failed burned CD when a data stream to the CD burner is interrupted long enough for the burner to write through all the data in its buffer.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the PCI bridge with parity detection system disclosed by Garbus ('027) such that it detects the use of the stunted 32-bit transfer mode instead of a 64-bit mode and raises a fault. This modification would have been obvious because many applications, such as CD burning and video capture require a minimum transfer rate, below which an error or decreased quality of service occurs.

19. As per claim 16, Garbus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the storage controlling apparatus according to claim 13, wherein said determining means determines that said modes do not agree with each other when a confirmation signal responding to said basic mode remains disabled at the time of executing said mode setting sequence (this is how PCI works, see PCI specification revision 2.3 section 3.8. REQ64 and ACK64 signals are sent by the receiver and transmitter. A lack of response with ACK64 on the part of the receiver causes the transmission to be downgraded to 32-bit mode).

20. As per claim 17, Garbus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the storage controlling apparatus according to claim 13, wherein said interface buses are PCI (Peripheral Component Interconnect) buses (as shown in Figure 2).

21. As per claim 20 this claim recites limitations found collectively in claims 16 and 17 and is rejected on the same grounds as claims 16 and 17.

22. As per claim 21, Garbus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the storage controlling apparatus according to claim 17, wherein said interface buses are 64-bit PCI buses (as disclosed by Garbus's ('027) use of PCI buses and PCI specification 2.3's use of 64-bt bus), said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8), said basic mode is said 64-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8, the 64-bit transfer mode provides additional bandwidth and is thus the preferred transfer mode); and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality (this limitation is made obvious by Sciforums and PC Hardware, in which a lower transfer rate results in an error or reduced quality of service), and notifies of said error notice (as is done with parity errors, see column 16 lines 47-51 and column 17 lines 19-26).

23. As per claim 24, this claim recites limitations found collectively in claims 20 and 21 and is rejected on the same grounds as claims 20 and 21.

24. As per claim 25, Garbus ('027) discloses an interface module for a storage controlling apparatus disposed between a disk unit and a host to control an access from said host to said disk unit (as shown in Figure 2, the PCI-to-PCI bridge contains a processor and resides between the host processors 1-4 and SCSI storage devices), said storage controlling apparatus comprising said interface module for controlling an interface with said disk unit or said host (SCSI devices attached to a PCI bus, as is shown in Figure 2, inherently require a interface unit to communicate on the PCI bus), a management module for generally managing the whole of said storage controlling apparatus (the PCI-to-PCI bridge 31 and its processor and interface generally manage the storage), and a bridge module for connecting said interface module and said management module to each other so that data can be transferred between said interface module and said management module (the PCI-to-PCI bridge 31 of Figure 2), said interface module comprising:

a first transfer processing unit for controlling data transfer between said interface module and said disk unit or said host (as shown in Figure 2, SCSI storage devices are connected via PCI bus to the bridge. A unit for controlling data transfer is inherently required because both SCSI and PCI protocols require unique handshaking protocols and that instructions sent be wrapped with message/packet overhead);

a second transfer processing unit for controlling data transfer between said interface module and said bridge module (as shown in Figure 2, a second interface is required to adapt the host processors 1-4 to the PCI bus);

said two transfer processing units being connected to each other in at least two different modes through an interface bus so that data can be transferred between said two transfer processing units (as shown in Figure 2, the system employs a PCI bus. The PCI specification revision 2.3 outlines the PCI use of 64-bit and 32-bit transfers. While 64-bit transfer is useful for products needing more bandwidth (PCI Specification section 3.8) 64-bit PCI devices are also capable of transfer in 32-bit mode for backward compatibility (PCI Specification section 3.8));

a determining means for determining whether or not an error occurs (column 8 lines 36-38, configuration registers of the bridge module hold error condition information); and

a notifying means for determining that transfer mode abnormality occurs and for notifying of an error notice (for example, column 17 lines 18-26, a parity error is detected and reported).

Garbus ('027) discloses a system that detects a bus parity error for data transmitting across the bridge. And while Garbus ('027) does feature a PCI device that would be obvious to have 64-bit and 32-bit transfer modes (according to the PCI specification, the 32-bit mode being used on the occurrence of a 64-bit mode setup discrepancy), Garbus ('027) does not expressly disclose the system wherein an error occurs upon a transfer mode discrepancy. In the claim language, Garbus ('027) does not expressly disclose the system wherein the PCI bus monitor reports an error upon determining that a basic

mode predetermined between said at least two different mode does not agree with a mode set in a mode setting sequence.

Sciforums teaches the use of a TV/Video Capture Card and that a lower level of service (dropped frames) can result from a number of system deficiencies, one of which is transfer rate.

PC Hardware in a Nutshell section 11.4 teaches that original CD burning suffered from buffer underrun errors that resulted in a failed burned CD when a data stream to the CD burner is interrupted long enough for the burner to write through all the data in its buffer.

25. As per claim 28, Garbus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the interface module for a storage controlling apparatus according to claim 25, wherein when a confirmation signal responding to said basic mode remains disabled at the time of executing said mode setting sequence, said determining means determines that said modes do not agree with each other (this is how PCI works, see PCI specification revision 2.3 section 3.8. REQ64 and ACK64 signals are sent by the receiver and transmitter. A lack of response with ACK64 on the part of the receiver causes the transmission to be downgraded to 32-bit mode).

26. As per claim 29, bus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the interface module for a storage controlling apparatus according to claim 25,

wherein said interface bus is a PCI (Peripheral Component Interconnect) bus (as shown in Figure 2, the PCI-to-PCI bridge bridges PCI buses).

27. As per claim 32, this claim recites limitations found collectively in claims 28 and 29, and is rejected on the same grounds as claims 28 and 29.

28. As per claim 33, Garbus ('027) in view of Sciforums and PC Hardware in a Nutshell discloses the interface module for a storage controlling apparatus according to claim 29, wherein said interface bus is a 64-bit PCI bus (as disclosed by Garbus's ('027) use of PCI buses and PCI specification 2.3's use of 64-bt bus), said at least two different modes are a 64-bit transfer mode and a 32-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8), said basic mode is said 64-bit transfer mode (as disclosed by PCI specification revision 2.3 section 3.8, the 64-bit transfer mode provides additional bandwidth and is thus the preferred transfer mode); and

when said determining means determines that said modes do not agree with each other, said notifying means determines that an inefficient transfer status occurs as said transfer mode abnormality (this limitation is made obvious by Sciforums and PC Hardware, in which a lower transfer rate results in an error or reduced quality of service), and notifies of said error notice (as is done with parity errors, see column 16 lines 47-51 and column 17 lines 19-26).

29. As per claim 36, this claim recites limitations found collectively in claims 32 and 33 and is rejected on the same grounds as claims 32 and 33.

Conclusion

The prior art made of record on accompanying PTO 892 form and not relied upon is considered pertinent to applicant's disclosure. Specifically, Asaad ('761) and Olarig ('810) teach PCI bus error handling and Byers ('393), Congdon ('296) and Smith ('694) teach systems with bus monitoring for fault detection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Schell whose telephone number is (571) 272-8186. The examiner can normally be reached on Monday through Friday 9AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS

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